

Abstracts

Known good die testing of wide S/C band power MMICs

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The testing process for power MMICs today is expensive and slow because it is done in a fixtured environment. The chip is usually diced up from a wafer, mounted on a carrier, and wire-bonded to an off-chip matching network (OCMN) before being tested. In this paper we demonstrate an integrated known-good-die testing solution at the wafer level, for a high-power S/C-band power amplifier. Fixtured and on-wafer results are compared.

 [Return to main document.](#)